IN THE SPECIFICATION

Please rewrite the paragraph on page 15, lines 9-24, as follows:

[0083] According to this embodiment, eighteen DRAMs 12 are ~~used,~~ used in a memory module 40, as shown in Fig. 14. That is to say, two DRAMs 12 are added to the DRAMs 12 of the first embodiment. These two added DRAMs 12 are stacked on a predetermined 1-ranked DRAM 12 and a predetermined 2-ranked DRAM 12 being adjacent thereto and paired therewith, whereby two units 41 of two DRAMs 12 stacked on each other are formed. One of the two units 41 of the stacked DRAMs 12 is provided on one face of the module substrate and a DRAM 12 is provided on the other face thereof so as to form a memory group. The other of the two units 41 of the stacked DRAMs 12 on one face of the module substrate and another DRAM 12 on the other face thereof also form another memory group. According to this configuration, active termination is performed in the DRAMs 12 on the other face of the module substrate. Fig. 16 shows simulation waveforms obtained by the above-described configuration. These simulation waveforms are a little blunter than the simulation waveforms shown in Fig. 9 but sharper than those shown in Figs. 11 and 13.

Please rewrite the paragraph on page 16, lines 17-28, as follows:

(0087] Fig. 18 shows wiring for taking out a CA signal of the stacked DRAMs 50. The CA signal of the stacked DRAMs 50 is taken out from an internal layer of the printed circuit board 51, as shown in Fig. 17A. Then, the CA signal is transmitted to a module substrate ~~61.~~ 61 through a ball terminal 57. Further, a CA signal of a DRAM 63 provided on an under face of the stacked DRAMs 50 is taken out from an internal layer of a package substrate 62 and transmitted to the module substrate ~~61.~~ 61 through a ball terminal 65. That is to say, the CA-signal wiring is

connected to both the DRAMs 50 and ~~63.~~ 63 through, for example, a via hole 66. Further, the stacked DRAMs 50 and the package substrate 62 are mounted on buffer materials 64 provided on both sides of the model substrate 61. Since the load on the CA-signal wiring connected to the stacked DRAMs 50 and the amount of time delay increase, the length of this CA-signal wiring should be reduced so as to be smaller than that of CA-signal wiring with a different configuration so as to synchronize the timing of this CA signal with the timing of other CA signals.

Please rewrite the paragraph on page 21, lines 11-25, as follows:

[0103] Fig. 24 shows a memory system whose configuration is different from that of the memory system shown in Fig. 6. This memory system has a memory controller 113, a memory module 110(1) including two DRAMs, a CAR, and a PLL ~~circuit,~~ circuit 111 with a termination resistor 112, and a memory module 110(2) including two DRAMs, a CAR, and a PLL ~~circuit.~~ circuit 111 with a termination resistor 112. As shown in this drawing, signal wiring between the memory controller 113 and the two DRAMs of the memory module 110(1) may have a T-branch structure. Signal wiring extending from the two DRAMs of the memory module 110(1) to the CAR thereof may also have a T-branch structure. Further, signal wiring between the memory controller 113 and the two DRAMs of the memory module 110(2) may have a T-branch structure. Signal wiring extending from the two DRAMs of the memory module 110(2) to the CAR thereof may also have a T-branch structure. According to the above-described configurations, the number of pins and wires of the memory controller 113 reduces, whereby the cost of manufacturing the memory controller 113 reduces.

Please rewrite the paragraph on page 22, lines 17-24, as follows:

[0107] As has been described, an ODT_CA signal is latched to the power-voltage level H or the ground level L according to the level of the ODT_CA signal. If the ODT_CA signal is latched to the power-voltage level H, an ODT_CA active terminal circuit 124 on the ground side is turned off. If the ODT_CA signal is latched to the ground level L, the ODT_CA active terminal circuit 124 on the power-voltage side is turned off. In both cases, no currents flow into the ODT_CA active terminal circuit 124 and the power consumption of the DRAM 121 reduces.